# Programable logic

## * Programable logic Array:

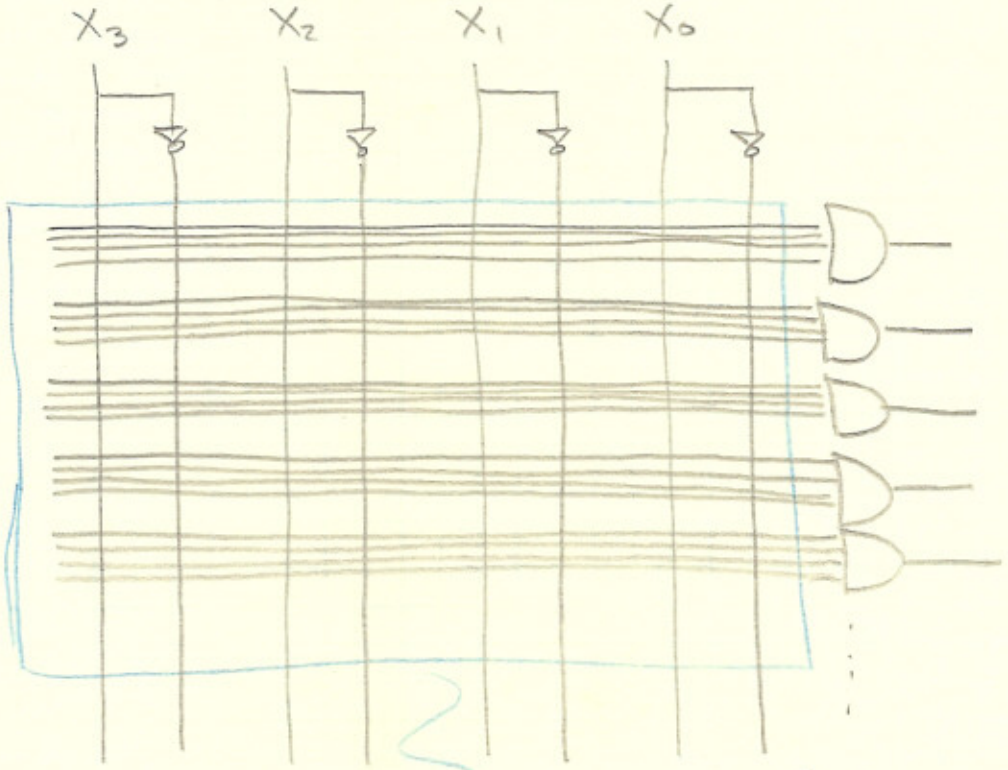
$$f_1 = X_3 \cdot \overline{X}_2 \cdot \overline{X}_1 \cdot X_0 + \overline{X}_3 \cdot \overline{X}_2 \cdot X_1 \cdot X_0$$

$$f_2 = X_3 \cdot \overline{X}_2 \cdot \overline{X}_1 \cdot X_0 + X_3 X_2 X_1 X_0$$

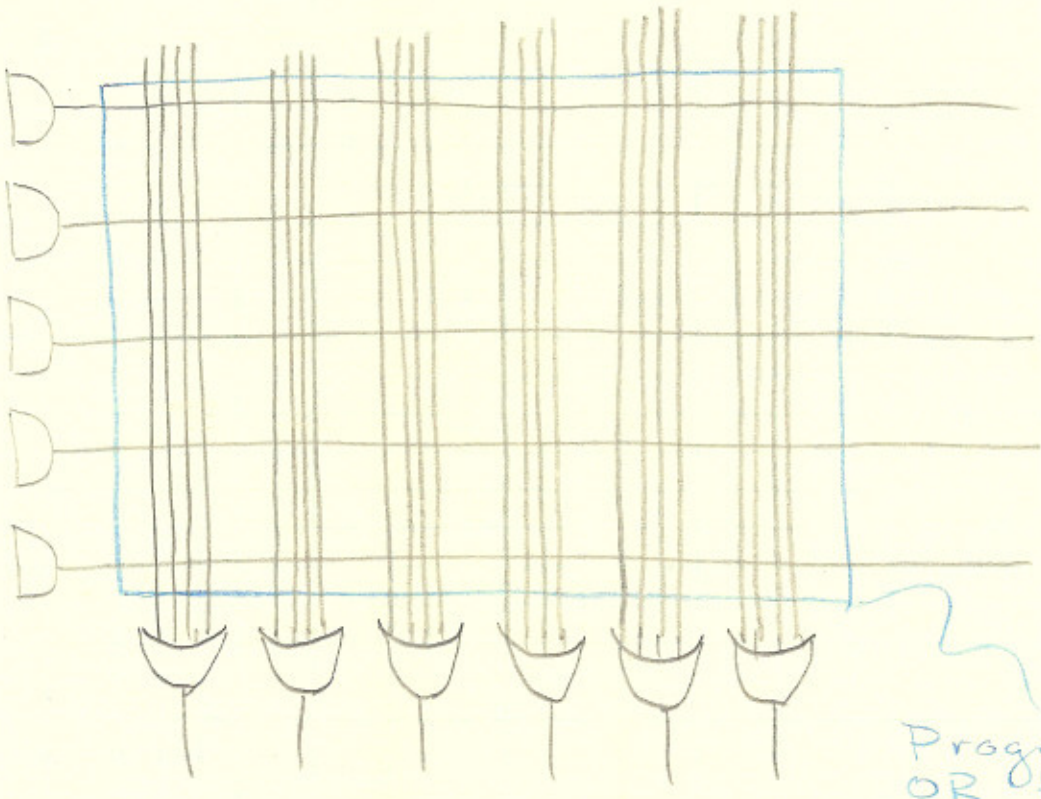
.....

$$f_8 = \overline{X}_3 \overline{X}_2 \overline{X}_1 \overline{X}_0 + X_3 \cdot X_2 \cdot X_1 (X_0 + \overline{X}_0)$$

$$= \overline{X}_3 \overline{X}_2 \overline{X}_1 \overline{X}_0 + X_3 X_2 X_1 X_0 + X_3 X_2 X_1 \overline{X}_0$$




**Note:** There must be an AND gate for every possible outcome; for 4 in i/p's there should be 16 out puts.



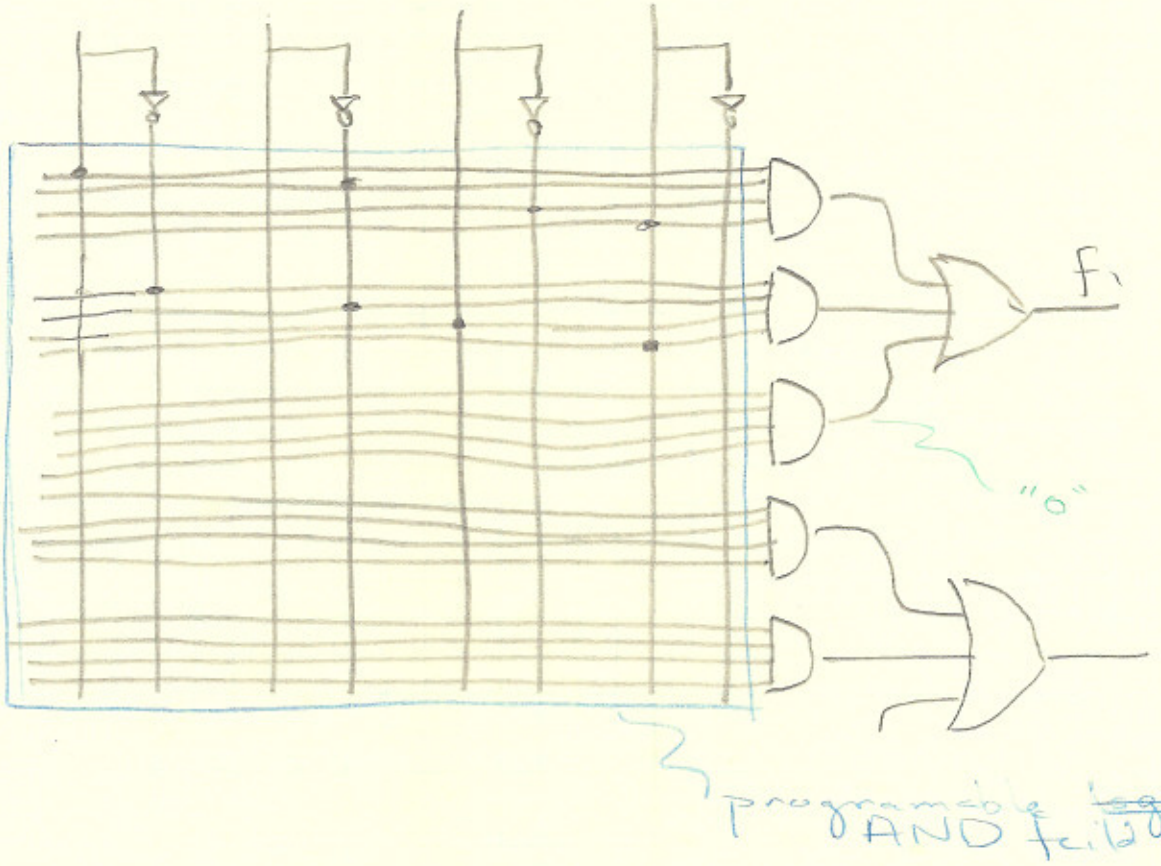

Note The number of OR gates depends on the capability of the system

By making connections at appropriate places in the two fields. The desired output circuit can be created.

* Programmable Array Logic (PAL)

$f_1 =$
$f_2 =$
$\vdots$
$f_8 =$

} same as last example




Note There are some serious disadvantages over the last device; we may end up with many more AND gates to perform the same task.

The main advantage is that there is only one feild to program.